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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/606,462	06/26/2003	Scott L. Michaelis	200205355-1	3496

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EXAMINER	
SUGENT, JAMES F	
ART UNIT	**PAPER NUMBER**
2116	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/606,462	MICHAELIS ET AL.	
	Examiner	Art Unit	
	James F. Sugent	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 February 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☒ Claim(s) *4,8 and 11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is sent in response to Applicant's Communication received February 13, 2007 for application number 10/606,462 originally filed June 26, 2003. The Office hereby acknowledges receipt of the following and placed of record in file: claims 1-23 are presented for examination.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 15-20 and 23 are rejected under 35 U.S.C. 102(b) as being anticipated by Walton et al. (U.S. Patent No. 7,103,639 B2) (hereinafter referred to as Walton).

As to claim 15, Walton discloses a partition of multiple partition computer system comprising: a plurality of processors (CPUs 302); firmware (PDH) comprising a reset code that resets a portion (cell) of the partition, wherein one processor of the plurality of processors ("monarch" processor) executes the reset code (Walton discloses the "monarch" processor within a cell managing booting and processor formation wherein PDH is a firmware device comprising booting code which is inclusive of initialization and reset; column 3, lines 5-12 and column 5, lines 35-47); and random access memory (cache within CM 304) that is not affected by the reset

code, that stores a list of addresses associated with the portion (Walton discloses a complex profile being created which is a "map" of the cell configuration which comprises location of devices assigned to a cell/partition which inherently would contain processor locations [addresses] and therefore register addresses; column 2, lines 7-15 and column 4, line 47 thru column 5, line 34).

As to claim 16, Walton further discloses the partition of claim 15, further comprising: read only memory that stores the firmware (column 3, lines 5-12).

As to claim 17, Walton further discloses the partition of claim 15, further comprising: a plurality of cells (see Fig. 1); wherein each cell comprises at least one processor of the plurality of processors (CPUs 302), and each cell comprises a reset register (state register) having an address that is on the list (column 5, line 55 thru column 6, line 20).

As to claims 18-20, they are directed to the partition of steps set forth in claim 17. Therefore, they are rejected for the same basis as set forth hereinabove.

As to claim 23, Walton disclose a computer readable medium having computer program logic recorded thereon for operating a partition of a multiple partition computer system, wherein the partition comprises a plurality of processors (CPUS 301), the computer program logic comprising: means for (101) building a list (data structure called complex profile) of reset register addresses associated with the plurality of processors (Walton discloses a complex profile being created which is a "map" of the cell configuration which comprises location of devices assigned to a cell/partition which inherently would contain processor locations [addresses] and therefore register addresses; column 2, lines 7-15 and column 4, line 47 thru column 5, line 34); means for (state registers via CM 304) placing each processor of the plurality of processors into a

known state (column 4, lines 47-63 and column 5, line 55 thru column 6, line 6); and, means for (CM 304) resetting the plurality of processors by writing a reset code (BIB) into their associated reset registers (column 4, lines 47-63 and column 5, line 55 thru column 6, line 20).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Walton (as cited above) in view of Harrington et al. (U.S. Patent Publication No. 2003/0236972 A1) (hereinafter referred to as Harrington).

As to claim 1, Walton discloses a method for resetting a partition of a multiple partition system, wherein the partition (see Fig. 1) comprises a plurality of processors (CPUs 302), the method comprising: executing, by one processor ("monarch" processor) of the plurality of processors, a reset code from firmware (PDH module) (Walton discloses the "monarch" processor within a cell managing booting and processor formation wherein PDH is a firmware device comprising booting code which is inclusive of initialization and reset; column 3, lines 5-12 and column 5, lines 35-47); building a list (data structure called complex profile) of reset register addresses associated with the plurality of processors (Walton discloses a complex profile being created which is a "map" of the cell configuration which comprises location of devices assigned to a cell/partition which inherently would contain processor locations [addresses] and

therefore register addresses; column 2, lines 7-15 and column 4, line 47 thru column 5, line 34); sending an interrupt (step 206 or 208) to the other processors of the plurality of processors (Walton discloses step 206 of Fig. 2 resetting a cell which necessitates an interrupt to the other processors of the cell upon reset. Also, Walton discloses the system "synchronizing" of cells in step 208 in Figs. 2 and 3 which also necessitates an interrupt; column 6, line 47 thru column 7, line 11); resetting the other processors (via CM 304) by writing a reset code to their associated reset registers (state register(s) associated with the cells) (column 4, lines 47-63 and column 5, line 55 thru column 6, line 20).

Walton fails to explicitly disclose resetting the one processor by writing to its associated reset register.

Harrington teaches a partitioned system wherein one processor of the partition (step 520 of Fig. 5) to process a warm reboot request (which sends out reset signals and interrupts to all of the other partition processors; paragraph 23 and paragraph 12) and then pass the control over to a service processor (135) to reset *all* of the processors in the partition and continue with the warm reboot (paragraphs 51 and 52). Therefore, the "one processor" of the partition resets all of the other processors and then a service processor (135) resets all of the processors to include the "one processor." Walton also teaches the system creating a list of resources (locating the resources) which is maintained by the system firmware (paragraph 4). Walton has the additional benefit of having a more reliable reboot process in a partition system ensuring all pending I/O requests within the system are halted/completed (paragraphs 12 and 13).

It would have been obvious to one of ordinary skill of the art having the teachings of Walton and Harrington at the time the invention was made, to modify method of Walton to

include the step of resetting the one processor as taught by Harrington. One of ordinary skill in the art would be motivated to make this combination of including the step of resetting the one processor after resetting all of the other processors in the partition in view of the teachings of Harrington, as doing so would give the added benefit of having a more reliable reboot process in a partition system ensuring all pending I/O requests within the system are halted/completed (as taught by Harrington above).

As to claim 2, Walton in combination with Harrington taught the method in claim 1, as shown above. Walton further teaches the method further comprising: storing the firmware on a read only memory (column 3, lines 5-12).

As to claim 3, Walton in combination with Harrington taught the method in claim 1, as shown above. Walton further teaches the method further comprising: storing the list of reset register addresses in random access memory ("caching" the complex profile within the CM 304; column 4, line 47 thru column 5, line 34).

As to claim 5, Walton in combination with Harrington taught the method in claim 1, as shown above. Harrington further teaches the method further comprising: requesting the execution of the reset code by a processor of the plurality of processors (paragraph 50).

As to claim 6, Walton in combination with Harrington taught the method in claim 1, as shown above. Harrington further teaches the method further comprising: requesting the execution of the reset code by an operating system of the multiple partition system (paragraphs 50 and 51).

As to claim 7, Walton in combination with Harrington taught the method in claim 1, as shown above. Harrington further teaches the method further comprising: requesting the

execution of the reset code by a firmware shell (hypervisor) of the multiple partition system (RTAS of hypervisor; paragraphs 42, 45 and 50).

As to claim 9, Walton in combination with Harrington taught the method in claim 1, as shown above. Harrington further teaches the method further comprising: flushing a cache associated with the one processor, after sending the interrupt (resetting all of the processors in the partition after running RTAS necessitates flushing the cache of the one processor; paragraphs 23, 50 and 51).

As to claim 10, Walton in combination with Harrington taught the method in claim 1, as shown above. Harrington further teaches the method further comprising: moving execution from main memory to read only memory (from the operating system to the hypervisor; paragraph 51).

As to claim 12, Walton in combination with Harrington taught the method in claim 1, as shown above. Walton further teaches the method wherein the partition comprises a plurality of cells, and each cell comprises at least one processor, the method further comprises: inventorying (updating the complex profile) the plurality of cells for resetting (column 5, lines 23-34).

As to claim 13, Walton in combination with Harrington taught the method in claim 1, as shown above. Walton further teaches the method wherein resetting the one processor occurs after resetting the other processors (paragraphs 50 and 51).

Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Walton and Harrington as applied to claim 1 above, and further in view of Applicant's Admitted Prior Art (hereinafter referred to as AAPA).

Applicant has admitted in the Background of the Invention that cells in a partition include Itanium Processor Family chips (paragraph 2).

Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Walton as applied to claim 15 above, and further in view of Harrington (as cited above).

As to claims 21, Walton fails to explicitly disclose the partition wherein the one processor is reset after the other processors of the plurality of processors are reset.

Harrington teaches a partitioned system wherein one processor of the partition (step 520 of Fig. 5) to process a warm reboot request (which sends out reset signals and interrupts to all of the other partition processors; paragraph 23 and paragraph 12) and then pass the control over to a service processor (135) to reset *all* of the processors in the partition and continue with the warm reboot (paragraphs 51 and 52). Therefore, the "one processor" of the partition resets all of the other processors and then a service processor (135) resets all of the processors to include the "one processor." Walton also teaches the system creating a list of resources (locating the resources) which is maintained by the system firmware (paragraph 4). Walton has the additional benefit of having a more reliable reboot process in a partition system ensuring all pending I/O requests within the system are halted/completed (paragraphs 12 and 13).

It would have been obvious to one of ordinary skill of the art having the teachings of Walton and Harrington at the time the invention was made, to modify method of Walton to include the step of resetting the one processor as taught by Harrington. One of ordinary skill in the art would be motivated to make this combination of including the step of resetting the one processor after resetting all of the other processors in the partition in view of the teachings of Harrington, as doing so would give the added benefit of having a more reliable reboot process in a partition system ensuring all pending I/O requests within the system are halted/completed (as taught by Harrington above).

Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Walton as applied to claim 15 above, and further in view of Applicant's Admitted Prior Art (hereinafter referred to as AAPA).

Applicant has admitted in the Background of the Invention that cells in a partition include Itanium Processor Family chips (paragraph 2).

Allowable Subject Matter

Claims 4, 8 and 11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: the limitation(s) found within these claims could not be found in further Examiner's search.

Response to Arguments

Applicant's arguments filed February 13, 2007 have been fully considered but they are not persuasive.

As to claim 15, Applicant first argues that Walton does not ever describe the resetting of the partition or a portion of the partition (Arguments; page 6, lines 1-2). The Examiner disagrees and stands by the rejection presented above as Walton does teach this limitation. Walton teaches a portion of a partition (cell) being reset (step 206) by a monarch processor (column 6, lines 49-57). Further, the Applicant even agrees with this in Arguments (page 6, lines 18-20).

Continuing with claim 15, Applicant continues to argue that Walton does not teach storing a list of addresses associated with the portion. Again, the Examiner disagrees. As rejected above, Walton teaches a data structure (complex structure) that stores "a map of the partition scheme" which is inclusive of addresses of the entire partition structure (column 4, line 64 thru column 5, line 22). Therefore, the Examiner stands by the rejection presented above for independent claim 15 under 35 USC § 102(b). Also, dependent claims 16-22 remain rejected based upon their dependence to rejected claim 15.

As to claim 23, Applicant argues that Walton does not comprise a means for building a list of reset register address locations associated with the plurality of processors. However, as argued above, Walton does teach creating a partition complex structure that creates a list of addresses of the entire partition structure. As a result, knowing the addresses of the processors within the partition inherently necessitates knowing the reset address locations. Furthermore, Applicant argues that Walton does not contain the limitation of resetting the plurality of processors by writing a reset code into their associated reset registers. Again, in order to reset a processor, a reset code (bit) is inherently written to the reset register of the processor to reset the processor. Therefore, for the reasons argued above and those similar limitations shared by claim 15, claim 23 remains rejected under 35 USC § 102(b).

As to claim 1, Applicant argues that neither Walton nor Harrington teaches executing by one of the processors, a reset code from firmware. However, Walton does teach this limitation and the Examiner stands by the rejection shown above. Walton teaches a firmware that is run on processor dependent hardware and cell microprocessors that boot and reset the cells of the partitions (column 3, lines 5-12 and column 5, lines 35-47).

Continuing with claim 1, the limitation of building a list of reset registers is argued on the same grounds shown hereinabove in re claim 15. Furthermore, the limitation of sending an interrupt to the other processors by writing a reset code is inherent to resetting processors such that an interrupt is inherently necessitated with resetting.

Therefore, the Examiner stands by the rejection presented above for independent claim 1 under 35 USC § 103(a). Also, dependent claims 2-14 remain rejected based upon their dependence to rejected claim 1.

In response to Applicant's argument that there is no suggestion to combine the references, the Examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, a recitation was taken directly from the secondary reference to provide the motivation.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to James Sugent whose telephone number is (571) 272-5726. The Examiner can normally be reached on 8AM - 4PM.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Rehana Perveen can be reached on (571) 272-3676. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at (866) 217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call (800) 786-9199 (IN USA OR CANADA) or (571) 272-1000.

James F. Sugent
Patent Examiner, Art Unit 2116
April 30, 2007

REHANA PERVEEN
SUPERVISORY PATENT EXAMINER
4/30/07